REMARKS

Claims 1-20 are all the claims presently pending in the application. Claims 1 and 8 have been amended to more particularly define the invention. Claims 1, 8, 14 and 19 are independent.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**" These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant notes that, notwithstanding any claim amendments herein or later during prosecution, that Applicant's intent is to encompass equivalents of all claim elements.

Claims 1 and 17 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Tao et al. (U.S. Patent No. 6,174,818) and claims 2-6 and 8-20 stand rejected under 35 U.S.C. § 103(a) as being obvious over Tao et al. in view of Ma et al. (U.S. Patent No. 5,783,101).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a method of forming a semiconductor device. The method includes providing a structure having a first critical dimension, forming a lithographic pattern on the structure, etching the structure with an O2 containing material to trim the first critical dimension to a second critical dimension and correcting an offset between a nested feature printed on the structure and an isolated feature printed on the structure. The second

critical dimension is smaller than the first critical dimension.

Conventional semiconductor forming methods have formed gates using many different types of techniques including a phase shift mask, an attenuated mask, a high numerical aperture monochromatic lithography tool, an extreme ultraviolet technique, etc. These techniques are problematic and include limitations. As shown in Figs. 1A - 1D, an anti-reflection coating (ARC) 102 is formed on a polysilicon layer 101 and a resist pattern 103 is formed on the ARC 102. The ARC 102 is etched via plasma etching (Fig. 1B) and the polysilicon 101 is etched via a gate reactive ion etching to achieve a good profile (Fig. 1C). Finally, the resist 103 and the ARC 102 are stripped to leave the gate situated on a gate oxide 104.

This conventional process is very complex. An ARC etch is critical to achieve line width bias and nested isolated offset and the polysilicon etch must achieve a good profile and stop on a thin oxide layer 104.

Additionally, it has been recognized that nested features are conventionally printed larger than isolated features with a negative photoresist process.

By contrast, the present invention provides a method for controlling the tolerance of isolated features by correcting an offset between a nested feature printed on the structure and an isolated feature printed on the structure. The present invention is capable of concentrating the etching upon the isolated features compared to the nested features using an RIE low pressure technique and of etching the nested features faster than the isolated features using a surface charging technique.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that the Tao et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by this reference.

The Tao et al. reference discloses a method of patterning a narrow gate electrode. In particular, the Tao et al. reference discloses providing a consumable hard mask of silicon oxynitride covered by a thin layer of silicon oxide during the etching of the polysilicon. The thicknesses of the two layers that make up the hard mask are chosen so that the structure also serves as an ARC for the photoresist coating immediately above it. A relatively thin layer for the photoresist is provided to improve resolution (Abstract). The invention disclosed by the Tao et al. reference combines the ARC function with substitution of a consumable hard mask for the photoresist mask during an etching step (col. 2, lines 37 - 41).

The Tao et al. reference does not teach or suggest correcting an offset between a nested feature printed on the structure and an isolated feature printed on the structure. Indeed, the Tao et al. reference only discusses etching of an isolated feature and does not teach or suggest anything regarding nested features.

The Examiner also alleges that the Ma et al. reference would have been combined with the Tao et al. reference to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Applicant submits that these references would not have been combined as alleged by the

Examiner. Indeed, the references are directed to different matters. Specifically, the Tao et al. reference is directed to forming a very narrow line through photolithography and etching (col. 1, lines 65-67) by combining the ARC function with substitution of a consumable hard mask for the photoresist mask during the etching step (col. 2, lines 37 - 41), whereas the Ma et al. reference is specifically directed to a high density plasma metal alloy etch process where the plasma source power frequency is reduced to a low RF frequency to reduce capacitive coupling from the plasma power source and to enable an increase in the plasma source power level (col. 3, lines 10-28). In other words, the Tao et al. reference is directed to improving semiconductor device resolution by providing a consumable hard mask while the Ma et al. reference is directed to the completely unrelated problem of providing a high density plasma metal alloy etch process.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner does not even support the combination by identifying a reason for combining the references.

Even assuming arguendo, that one of ordinary skill in the art would have been motivated to combine these references, even if combined, the combination would not teach or suggest each and every element of the claimed invention.

The Ma et al. reference, like the Tao et al. reference, does not teach or suggest correcting an offset between a nested feature printed on the structure and an isolated feature printed on the structure. As noted above, the claimed invention includes innovative techniques to correct the offset between a nested feature and an isolated feature. Neither of the applied references teach or suggest this feature. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

The Office Action objects to the drawings. This Request for Reconsideration encloses a Submission of Proposed Drawing Corrections which corrects Figs. 1A - 1D to recite "Prior Art" in accordance with Examiner Sagar's helpful suggestion. Applicants respectfully request withdrawal of this objection.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-20, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 11/12/02

James E. Howard, Esq.
Reg. No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please amend claims 1 and 8 to read as follows:

1. (Amended) A method of forming a semiconductor device, comprising:

providing a structure having a first critical dimension;

forming a lithographic pattern on said structure; [and]

etching said structure with an O2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension; and

correcting an offset between a nested feature printed on said structure and an isolated feature printed on said structure.

8. (Amended) A method of trimming a conductor on a substrate, comprising:

providing a conductor having a first critical dimension;

forming a lithographic pattern on said conductor; [and]

etching said conductor with an O2-containing material to trim said first critical dimension to a second critical dimension, said second critical dimension being smaller than said first critical dimension; and

correcting an offset between a nested feature printed on said structure and an isolated feature printed on said structure.